Conquering IC Virtual Prototyping: Pre-Silicon Architecture and Verification to Post-Silicon Correlation

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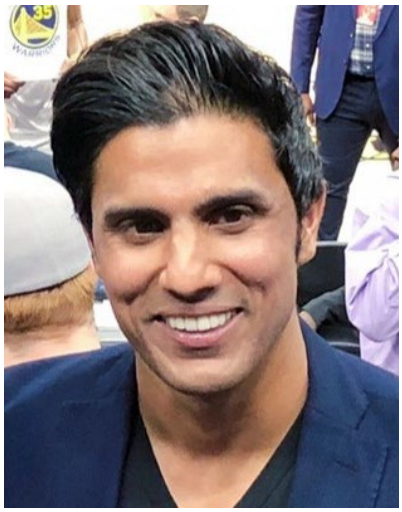
Abstract - Signal integrity has entered a phase of maturity after the rise of several generations of high-speed link designs across consumer and data center products. No longer is it considered to be "black magic" as many signal and power integrity methods and analyses have been integrated into product development cycles to avoid costly project delays due to chip, package, or PCB spins. Part of the proliferation can also be attributed to the growth in capability of commercially available EM tools and expansion in compute resources. While some of the signal integrity fundamentals and theory have existed for some time now, there are a lot of unique upcoming challenges in building chips and designing the systems for tomorrow. This talk will explore some of the unique signal and power integrity problems which arise from larger trends in the semi-conductor industry including IC disaggregation, circumventing memory bottlenecks along with overall concerns about gross margins from a product cost perspective. These all pose unique challenges that push the boundaries of the signal and power integrity solution space and force innovation. A case study on GDDR6x will be presented to show the innovation from early-stage architectural studies to post-silicon correlation.

Biography:



Sunil Sudhakaran is currently a Distinguished Engineer at NVIDIA in the Mixed Signal group. He received the B.S. degree in Computer Engineering and Minor in Business from the University of Wisconsin Madison in 2004 and the M.S. degree in Electrical Engineering from Stanford University in 2006. He joined the Signal Integrity group at NVIDIA in 2006 and led the team in 2013. He has made significant contributions across NVIDIA product lines and authored several publications and patents. He received the IEEE EPEPS Best Paper Award in 2016 and co-authored a few DesignCon Best Paper award winning papers. He has recently transitioned to a part-time role @ NVIDIA as he is returning to Stanford University to complete his PhD in Electrical Engineering.