224 Gbps and More-than-Moore

Mike Peng Li, Intel

Abstract - Moore's law continues to drive the advancements of density, power, and performance for SOCs (e.g., CPU, GPU, FPGA, ASIC/ASSP) via transistor feature size and interconnect shrinkage, as well as switch speed increases. In the near future, transistors and semiconductors will enter the atomic size: Angstrom (Å). Meanwhile, Moore's law continues to drive the SERDES I/O speed doubling at a pace around every 3 years, and soon will reach 224 Gbps per lane speed. In this talk, we will review the SERDES I/O speed advancement path and highlight the end-to-end challenges at 224 Gbps, from silicon, to package, to PCB/connectors, and associated solution options. Furthermore, we will discuss how Moore's law and atomic Angstrom process nodes will enable 224 Gbps data rate to achieve the desired power, performance, and density via More-Moore, and More-than-Moore.

Biography:

Dr. Peng (Mike) Li is an Intel Fellow and the technologist for high-speed I/O and interconnects at Intel Corporation. He serves as Intel's technical expert and adviser in high-speed I/O and link technology; standards; SerDes architecture; electrical and optical signaling and interconnects; silicon photonics integration; optical field-programmable gate arrays (OFPGAs); and high-speed simulation, debug and test for jitter, noise, signaling and power integrity, from deign validation to high-volume manufacturing (HVM).

Li joined Intel in 2015 with the acquisition of Altera Corp., where he had held a similar role since 2012. Before joining Altera in 2007, Li spent nearly a decade at Wavecrest Corp. culminating in his seven-year tenure as chief technology officer (CTO). He began his career in 1991 as a post-doctorate researcher on high-energy astrophysics at the Space Sciences Laboratory at the University of California, Berkeley.

A distinguished scientist and technologist, Li has contributed extensively to standards during his industry career including PCI Express, Ethernet, Optical Internetworking Forum (OIF), JEDEC, Fibre Channel, and SATA/SAS. He has also published widely, including >120 referred papers, >40 patents, five books and book chapters on jitter and high-speed architecture, testing, modeling, and analysis.

Li earned a bachelor's degree in space physics from the University of Science and Technology of China in Hefei, China; a master's degree in physics and a master's degree in electrical and computer engineering, both from the University of Alabama in Huntsville (UAH); and a Ph.D. in physics, also from UAH. Li was named an IEEE Fellow in 2012, an Altera Fellow (2012), an Intel Fellow (2015), and Engineer of the year (2018, Designcon). He served as the BOD member for OIF since 2018. He has been elected as an affiliated professor at the Department of Electrical Engineering, University of Washington, Seattle, since 2010.

Packaging and new ways to stay ahead of “The Law” in High Performance Computing

Bradley (Brad) Mcredie, AMD

Abstract - The path to exascale computing is the path of cost/performance optimization. In fact, cost/performance optimization has been a constant in IT. However, the definition of cost and performance has evolved over the past two decades. What will it take to truly drive performance and add value in today's HPC market?

3D stacking and other advanced packaging technologies are truly a game changers for Moore's Law scaling--with the ability to achieve generational node performance not by silicon scaling, but by advanced packaging innovations. Join industry veteran Brad McCredie, Vice President for the Data Center GPU and Accelerated Processing business at AMD, as he shares key insights and innovation strategies around advanced packaging technologies and more to drive to exascale computing and beyond.

Biography:

Dr. Bradley (Brad) McCredie joined AMD in June 2019 as Vice President Data Center GPU and Accelerated Processing running the Data Center GPU and Accelerated Processing Business driving AMDs data center strategy covering Data Center GPU and CPU + GPU solutions.

Prior to joining AMD, Brad was an IBM Fellow and Vice President of IBM Power Systems Development. In that role, Brad was responsible for system hardware, software, solutions, and ecosystem development teams, driving advanced technologies to support customer needs. During his tenure at IBM, Brad worked on the development of IBM POWER2 - POWER9 processor families. Additionally, Brad helped to lead the creation of the OpenPOWER foundation, an independent group of global technologists who encourage the adoption of an open server architecture for computer data centers.

Dr. McCredie holds bachelor’s, master’s and doctorate degrees in electrical and computer engineering from the University of Illinois at Urbana-Champaign.