Preliminary Program (Advanced Program to be posted 9/15/2021)

Sunday, October 17, 2021

Session S-I

7:50 - 8:00 Conference Kick-Off

IEEE EPEPS 2021 Welcome by Conference General Co-Chair Jose A. Hejase -NVIDIA Corporation-

Session S-II

8:00 - 9:00 Tutorial I

Title: The HIR - Packaging, Heterogeneous Integration, and High Performance Computing
Speaker: Dale Becker -IBM Corporation-

Session S-III

8:00 - 9:00 Tutorial II

Title: Interposer Analysis: Challenges and Solutions for Efficient 3D EM Extraction
Speaker: Amir A. Asif -Cadence-

Session S-IV

9:00 - 10:00 Tutorial III

Title: Addressing EM Simulation Challenges for IC-Package-Board Problems
Speakers: Feng Ling - Xpeedic -; Jonatan Aronsson -CEMWorks, Inc.-

Session S-V

9:00 - 10:00 Tutorial IV

Title: Tutorial on Electrical Characterization and Measurement for Electronic Packaging
Speakers: Heidi Barnes -Keysight Technologies-; Michael J. Hill -Intel Corporation-; Wui-Weng Wong -AMD-

Session S-VI

10:00 - 10:10 Break

Session S-VII

10:10 - 11:10 Tutorial V

Title: Analysis and optimization of SerDes interfaces running at 100Gbps per lane
Speakers: Cristian Filip -Siemens EDA-; Daniel De Araujo -Siemens EDA-

Session S-VIII

10:10 - 11:10 Tutorial VI

Title: Package Design Considerations for Enabling High Volume Manufacturing Test
Speaker: Mike Ryan -Intel Corporation-

Session S-IX

11:10 - 12:10 Tutorial VII

Title: Analysis of Direct-to-Chip-Package 224G Channels
Speaker: Michael Rowlands -Amphenol-

Session S-X

11:10 - 11:50 Tutorial VIII

Title: Packaging challenges for mobile and beyond, an industry perspective
Speakers: Gerardo Romo Luevano -Qualcomm-; Joonsuk Park -Qualcomm-

Session S-XI

12:10 - 12:50 Annual IEEE EDMS Meeting

Annual IEEE EDMS Report and Discussion
Meeting Leader: Dale Becker -IBM Corporation-

Session S-XII

12:50 - 1:00 Day 1 Wrap Up

Day 1 Wrap Up by Conference Co-Chair Zhen Peng -University of Illinois at Urbana Champaign-

Monday, October 18, 2021

Session M-I

7:50 - 8:00 **Day 2 Welcome**

Day 2 Welcome by Conference Co-Chair Zhen Peng -University of Illinois at Urbana Champaign-

Session M-II

8:00 - 9:00 **Keynote I**
Chairs: Zhen Peng, University of Illinois at Urbana-Champaign

Title: 224 Gbps and More-than-Moore
Speaker: Mike Peng Li -Intel Corporation-

Session M-III

9:00 - 10:20 **High Speed Links I**
Chairs: TBD, TBD

- M-III.1. **Crosstalk-included PAM-4 Worst Eye Diagram Estimation Method for High-speed Serial Links**

Jinwook Song*, Youngmin Ku*, Jonggyu Park*, Joungho Kim+, Hyunwook Park+, Jihun Kim+, Minsu Kim+, Keunwoo Kim+, Boogyo Sim+, Daehwan Lho+, Taein Shin+, Keeyoung Son+

*Samsung Electronics, +Korea Advanced Institute of Science and Technology (KAIST)

- M-III.2. **Effect of Sampling Method on the Regression Accuracy for a High-Speed Link Problem**

Hanzhi Ma*, Cangellaris Andreas+, Xu Chen+

*Zhejiang University, +University of Illinois at Urbana-Champaign

- M-III.3. **Novel Approach to Voltage Adjustment of Low-noise Signaling in Power over Coax Circuits**

Yutaka Uematsu*, Soshi Shimomura*, Yasuhiro Ikeda*, Hidetatsu Yamamoto+, Hideyuki Sakamoto*

*Hitachi, Ltd., +Hitachi Astemo Ltd.

- M-III.4. **Parallel Bayesian Active Learning using Dropout for Optimizing High-Speed Channel Equalization**

Hakki Torun[*], Junyan Tang[+], Madhavan Swaminathan[*], Xianbo Yang[+], Pavel Paladhi[+], Yanyan Zhang[+], Wiren Becker[+], Jose Hejase[**]

[*]Georgia Institute of Technology, [+]IBM Corporation, [**]Nvidia Corporation

Session M-IV

9:00 - 10:20 **Advanced CAD I**
Chairs: TBD, TBD

- M-IV.1. **Statistical Crosstalk Analysis via Probabilistic Machine Learning Surrogates**

Paolo Manfredi, Riccardo Trinchero

Politecnico di Torino

- M-IV.2. **Bivariate Macromodeling with Passivity Constraints**

Tommaso Bradde, Alessandro Zanco , Stefano Grivet-Talocia

Politecnico di Torino

- M-IV.3. **Fast Extraction of Per-Unit-Length Parameters of Hybrid Copper-Graphene Interconnects via Generalized Knowledge Based Machine Learning**

Suyash Kushwaha[*], Amir Attar[+], Riccardo Trinchero[+], Flavio Canavero[+], Rohit Sharma[*], Sourajeet Roy[**]

[*]Indian Institute of Technology Ropar, [+]Politecnico di Torino, [**]Indian Institute of Technology Roorkee

- M-IV.4. **Closed-Form Evaluation of Michalski-Zheng's Mixed Potential Green's Function in Unbounded Layered Media Using Spectral Differential Equation Approximation Method**

Vladimir Okhmatovski, Xinbo Li

University of Manitoba

Session M-V

10:20 - 10:30 **Break**

Feature Video
Sponsored by: Intel Corporation (Gold Sponsor)

Session M-VI

10:30 - 12:00 Sponsor Virtual Booths

Product exhibit by: Amphenol, Cadence, Keysight Technologies, Siemens EDA, Xpeedic

Session M-VII

12:00 - 1:00 **Power Integrity and Power Distribution Networks I**
Chairs: TBD, TBD

- M-VII.1. **Pre-driver Modeling and Jitter Estimation under Power Supply Noise**

Malek Souilem[*], Hamdi Belgacem[+], WAEL DGHAIS[+], Jai Narayan Tripathi[**]

[*]National Engineering School of Sousse, University of Sousse, [+]Higher Institute of Applied Sciences and Technology of Sousse, University of Sousse, [**]Department of Electrical Engineering, Indian Institute of Technology Jodhpur, Jodhpur

- M-VII.2. **Distributed Nonlinear Shielding in Power Delivery Networks on Printed Circuit Boards**

Torben Wendt[*], Marco De Stefano[+], Cheng Yang[*], Stefano Grivet-Talocia[+], Christian Schuster[*]

[*]Hamburg University of Technology, [+]Politecnico di Torino

- M-VII.3. **Deep Reinforcement Learning Framework for Optimal Decoupling Capacitor Placement on General PDN with an Arbitrary Probing Port**

Haeyeon Kim[*], Hyunwook Park[*], Minsu Kim[*], Seonguk Choi[*], Jihun Kim[*], Joonsang Park[*], Seongguk Kim[*], Subin Kim[+], Joungho Kim[*]

[*]Korea Advanced Institute of Science and Technology (KAIST), [+]Global Technology Center (GTC), Samsung Electronics Co., Ltd

Session M-VIII

12:00 - 1:00 **Package Design Methods**
Chairs: TBD, TBD

- M-VIII.1. **Deep Reinforcement Learning-based Pin Assignment Optimization of BGA Packages considering Signal Integrity with Graph Representation**

Joonsang Park, Minsu Kim, Seongguk Kim, Keeyoung Son, Taein Shin, Hyunwook Park, Seonguk Choi, Haeyeon Kim, Keunwoo Kim, Joungho Kim

Korea Advanced Institute of Science and Technology (KAIST)

- M-VIII.2. **A Scalable In-Context Design and Extraction Flow for Heterogeneous 2.5D Chiplet-Package Co-Optimization**

MD Arafat Kabir*, Dusan Petranovic+, Yarui Peng*

*University of Arkansas, +Mentor Graphics

- M-VIII.3. **Co-optimizing signaling protocol with semiconductor and packaging technology**

Bapi Vinnakota*, Shahab Ardalan+, Subramanian Iyer**, Krutikesh Sahoo**

*Broadcom Corporation, Santa Clara, CA, +Ayar Labs, Santa Clara, CA, **University of California, Los Angeles, CA

Session M-IX

1:00 - 1:10 Day 2 Wrap Up

Day 2 Wrap Up by Conference General Co-Chair Jose A. Hejase -NVIDIA Corporation-

Tuesday, October 19, 2021

Session T-I

7:50 - 8:00 **Day 3 Welcome**

Day 3 Welcome by Conference General Co-Chair Jose A. Hejase -NVIDIA Corporation-

Session T-II

8:00 - 9:00 **Keynote II**
Chairs: Jose A. Hejase, NVIDIA Corporation

Title: Packaging and new ways to stay ahead of -The Law- in High Performance Computing
Speaker: Brad (Bradley) Mcredie -AMD-

Session T-III

9:00 - 10:20 **High Speed Links II**
Chairs: TBD, TBD

- T-III.1. **BGA Routing Impact on High-Speed Signals**

  Gregory Pitner[*], Wade Smith[*], Mallikarjun Vasa[+], Raymond Pavlak[+], Douglas Winterburg[+] — [*]Ansys, [+]Dell

- T-III.2. **Design and Analysis of HDMI 2.1 Connector for Crosstalk Reduction using Tabs and Inverse Tabs**

  Park Gapyeol[*], Son Kyungjune[*], Kang Hyungmin[*], Sim Boogyo[*], Kim Seongguk[*], Shin Taein[*], Kim Keunwoo[*], Son Keeyoung[*], Kim Jinyoung [+], Kim Joungho[*], Park Joonsang[*], Daehwan Lho[*], Park Hyunwook[*] — [*]Korea Advanced Institute of Science and Technology (KAIST), [+]Korea Electric Terminal Co. Ltd (KET)

- T-III.3. **Layout Technique for Space Reduction of DC-Block Capacitors**

  Juan Martinez, Kerry Ford — IBM

- T-III.4. **Fast and Accurate Modeling of PCB Differential Trace Skew Compensation using ML**

Jay Reddy*, James Pingenot+, Daniel de Araujo+, Cristian Filip+, Swagato Chakraborty+, Chuck Ferry+, James Mobley*, Doug Wallace*, Varun Gorti**, Adam Klivans**, David Pan**

*Dell Technologies, +Siemens EDA, **UT Austin

Session T-IV

9:00 - 10:20 **Advanced CAD II**
Chairs: TBD, TBD

- T-IV.1. **Quantum Method of Moments for Characterization of Interconnects**

Vladimir Okhmatovski, Christopher Phillips — University of Manitoba

- T-IV.2. **A Fast Surface Integral Method for the Wideband Frequency Analysis of Interconnect Networks**

Shashwat Sharma, Piero Triverio — University of Toronto

- T-IV.3. **On the Statistical Analysis of Space-Time Wave Physics in Complex Enclosures**

Shen Lin, Zhen Peng — University of Illinois at Urbana-Champaign

- T-IV.4. **A Basis-Free Loop-Star Preconditioned Reduced-Domain Layered-Medium Integral-Equation Solver**

Yi-Ru Jeong, Ali E. Yilmaz — The University of Texas at Austin

Session T-V

10:20 - 10:30 **Break**

Feature Video
Sponsored by: NVIDIA Corporation (Gold Sponsor)

Session T-VI

10:30 - 11:30 **30 Years of EPEPS Panel**

Chairs: Kemal Aygun, Intel Corporation

Panelists --> TBD

Session T-VII

11:30 - 12:00 **IEEE EPS TC-EDMS Presentation**
Chairs: TBD, TBD

TC-EDMS Packaging Benchmarks Committee Progress Report 2021
by
Ali Yilmaz -University of Texas at Austin-
Fei Guo -AMD-

Session T-VIII

12:00 - 1:00 **Power Integrity and Power Distribution Networks II**
Chairs: TBD, TBD

- T-VIII.1. **Deep Reinforcement Learning-based Power Distribution Network Structure Design Optimization Method for High Bandwidth Memory Interposer**

  Hyunwoong Kim, Kyunghwan Song, Jongwook Kim, Dongryul Park, Jangyoung Ahn, Keunwoo Kim, Seungyoung Ahn — Korea Advanced Institute of Science and Technology

- T-VIII.2. **Automatic Package Router for Power Delivery Network**

  Ryan Coutts, Abinash Roy, Mali Nagarajan, Vaishnav Srinivas, Paul Penzes — Qualcomm Technologies Inc.

- T-VIII.3. **Inverse Design of Power Delivery Networks using Invertible Neural Networks**

  Osama Waqar Bhatti, Nikita Ambasana, Madhavan Swaminathan — Georgia Institute of Technology

Session T-IX

12:00 - 1:00 **Signal Integrity Analysis Methods**
Chairs: TBD, TBD

- T-IX.1. **High Speed Receiver ModelingUsing Generative Adversarial Networks**

  Priyank Kashyap, Pitts Wallace, Dror Baron, Chau-Wai Wong, Tianfu Wu, Paul Franzon — North Carolina State University

- T-IX.2. **Evaluation of S-Parameters Similarity with Modified Hausdorff Distance**

  Yuriy Shlepnev — Simberian, Inc.

- T-IX.3. **Sequential Policy Network-based Optimal PassiveEqualizer Design for an Arbitrary Channel of HighBandwidth Memory using Advantage Actor Critic**

  Joungho Kim, Seonguk Choi, Minsu Kim, Hyunwook Park, Keeyoung Son, Seongguk Kim, Jihun Kim, Joonsang Park, Haeyeon Kim, Taein Shin, Keunwoo Kim — Korea Advanced Institute of Science and Technology

Session T-X

1:00 - 1:10 **Day 3 Wrap Up**

Day 3 Wrap Up by Conference Co-Chair Zhen Peng -University of Illinois at Urbana Champaign-

Wednesday, October 20, 2021

Session W-I

7:50 - 8:00 **Day 4 Welcome**

Day 4 Welcome by Conference Co-Chair Zhen Peng -University of Illinois at Urbana Champaign-

Session W-II

8:00 - 9:00 **Invited Presentation**
Chairs: Jose A. Hejase, NVIDIA Corporation

Title: Conquering High-Speed Link Virtual Prototyping: Pre-Silicon Architecture and Verification to Post-Silicon Correlation
Speaker: Sunil Sudhakaran -NVIDIA Corporation-

Session W-III

9:00 - 10:20 **Signal and Thermal Integrity**
Chairs: TBD, TBD

- W-III.1. **Broadside-Coupled Differential Routing In Package Via Pin-Field Design**

  Yanyan Zhang, Lloyd Walls, Mahesh Bohra, Junyan Tang, Xianbo Yang, Dale Becker, Daniel Dreps — IBM

- W-III.2. **Signal Integrity Analysis of High Speed Channel considering Thermal Distribution**

  Keeyoung Son, Seongguk Kim, Minsu Kim, Daehwan Lho, Keunwoo Kim, Hyunwook Park, Gapyeol Park, Joungho Kim — KAIST

- W-III.3. **Far End Crosstalk Mitigation of Differential High Speed Interconnects Within Printed Circuit Board Via Fields**

  Junyan Tang[*], Xianbo Yang[*], Jose Hejase[+], Mahesh Bohra[*], Yanyan Zhang[*], Xiaomin Duan[*], Dierk Kaller[*], Wiren Becker[*], Daniel Dreps[*] — [*]IBM, [+]Nvidia

- W-III.4. **Modeling and Signal Integrity Analysis of Mounting Pad with Layer-cutting to reduce Impedance Mismatch for Dual-In-Line Memory Module (DIMM)**

Hyunwoong Kim[*], Jongwook Kim[*], Kyunghwan Song[*], Seonghi Lee[*], Keunwoo Kim[*], Seongguk Kim[*], Daehwan Lho[*], Hyunsik Kim[+], Seungyoung Ahn[*], Minho Park[+]

[*]Korea Advanced Institute of Science and Technology, [+]SK Hynix

Session W-IV

9:00 - 10:20 **Machine Learning for High Speed Links**
Chairs: TBD, TBD

- W-IV.1. **Invertible Neural Networks for High-Speed Channel Design & Parameter Distribution Estimation**

Osama Waqar Bhatti[*], Majid Ahadi Dolatsara[*], Madhavan Swaminathan[*], Xianbo Yang[+], Pavel Roy Paladhi[+], Dale Becker[+]

[*]Georgia Tech, [+]IBM Systems USA

- W-IV.2. **Imitation Learning for Simultaneous Escape Routing**

Minsu Kim[*], Hyunwook Park[*], Keeyoung Son[*], Seongguk Kim[*], Haeyeon Kim[*], Jihun Kim[*], Jinwook Song[+], Youngmin Ku[+], Jounggyu Park[+], Joungho Kim[*]

[*]KAIST, [+]Samsung Electronics

- W-IV.3. **PAM-4 based PCIe 6.0 Channel Design Optimization Method using Bayesian Optimization**

Seonguk Choi[*], Keeyoung Son[*], Joonsang Park[*], Haeyeon Kim[*], Jinwook Song[+], Youngmin Ku[+], Jihun Kim[*], Hyunwook Park[*], Minsu Kim[*], Seongguk Kim[*], Jonggyu Park[+], Joungho Kim[*]

[*]Korea Advanced Institute of Science and Technology (KAIST), [+]Samsung Electronics

- W-IV.4. **Prediction of De-embedded Eye Height/Width Parameters using Machine Learning in High Speed Serial Link Characterization**

Mohit Goyal[*], Maneesh pandey[+], Sharad kumar[**], Rohit Sharma[+]

[*]Intel India, [+]IIT Ropar, [**]NXP

Session W-V

10:20 - 10:30 Break

Feature Video
Sponsored by: Qualcomm (Gold Sponsor)

Session W-VI

10:30 - 12:00 Sponsor Student Recruiting Event

Hosted by: IBM Corporation, Intel Corporation, NVIDIA Corporation, Qualcomm

Session W-VII

12:00 - 1:00 **Measurement Correlation and Enhancement Techniques**
Chairs: TBD, TBD

- W-VII.1. **Impact of Copper Pour on Crosstalk: Measurement and Simulation Correlation**

  Aditya Rao[*], Saish Sawant[+], Eric Bogatin[*], Melinda Piket-May[*] — [*]University of Colorado, Boulder, [+]Keysight Technologies

- W-VII.2. **Power Delivery Noise Measurement Technique for Xeon Validation**

  Felipe de J. Leal-Romo, Daniel Mauricio Garcia-Mora, Benjamin Mercado-casillas, Jayashree Kar, Jorge Armando Ortiz-Ramirez — Intel corp.

- W-VII.3. **Enhancements to the Non-Invasive Current Estimation Technique Through Ground Isolation**

  Chad Smutzer, Jordan Keuseman, Christopher White, Clifton Haider, Barry Gilbert — Mayo Clinic - SPPDG

Session W-VIII

12:00 - 1:00 **Signal and Power Integrity Methodology Investigations**
Chairs: TBD, TBD

- W-VIII.1. **Modeling Finite Dielectric Structures Embedded in Layered Medium for IC Packages and Boards**

Giacomo Bianconi, Swagato Chakraborty — Siemens EDA

- W-VIII.2. **Eye Comparison Between Unencoded and 128b/130b-encoded NRZ Signals**

Pei-Yang Weng[*], Ching-Huei Chen[+], James Chen[+], Evelyn Kuo[+], Eva Lin[+], Paul Chu[+], Chun-Lin Liao[+], Bhyrav Mutnury[+], Tzong-Lin Wu[*]

[*]National Taiwan University, [+]DellEMC Infrastructure Solution Group

- W-VIII.3. **Evaluation of Support Vector Machines for PCB based Power Delivery Network Classification**

Morten Schierholz, Youcef Hassab, Cheng Yang, Christian Schuster

Institut fuer Theoretische Elektrotechnik, Hamburg University of Technology (TUHH)

Session W-IX

1:00 - 1:10 Conference Wrap Up

IEEE EPEPS 2021 Conference Wrap Up by Conference Co-Chairs Jose A. Hejase -NVIDIA Corporation- & Zhen Peng -University of Illinois at Urbana Champaign-