# IEEE EPEPS 2026 Program

Embassy Suites Fort Worth Downtown, October 18–21, 2026 · Updated October 18, 2026

SCAN ME
Proceedings

## Sunday, October 18, 2026

### Session 1: Welcome Remarks
9:00 AM – 9:10 AM · Synergy 1 · Chair: Xu Chen

### Session 2: IEEE EPS Distinguished Lecture
9:10 AM – 10:10 AM · Synergy 1 · Chair: Xu Chen

9:10 AM **Advanced Packaging for High-Speed Chiplet Interconnects: Technologies, Methodologies, and Standards**
*Kemal Aygun* (Intel)

### Session 3: Tutorial 2
10:10 AM – 11:10 AM · Synergy 1 · Chair: Xu Chen

10:10 AM **From Co-Packaged Optics to Co-Packaged Photonic Systems**
*Mohamed Elkabbash* (University of Arizona)

**11:10 AM – 11:30 AM · Coffee Break · Pre-Function (5th Floor)**

### Session 4: Tutorial 3
11:30 AM – 12:30 PM · Synergy 1 · Chair: Xu Chen

11:30 AM **Signal and Power Integrity Analysis for Next-Generation 2.5D/3D Advanced Packaging**
*Feng Ling* (Xpeedic)

**12:30 PM – 2:00 PM · Lunch Break (Not Provided)**

### Session 5: Tutorial 4
2:00 PM – 3:00 PM · Synergy 1 · Chair: Rajen Murugan

2:00 PM **Opportunities in NeuroAI: A Hardware-Software Co-Design Perspective**
*Abhronil Sengupta* (The Pennsylvania State University)

### Session 6: Tutorial 5
3:00 PM – 4:00 PM · Synergy 1 · Chair: Rajen Murugan

3:00 PM **Gaussian Processes for Data-Efficient Uncertainty Quantification, Optimization and Active Learning**
*Paolo Manfredi* (Politecnico di Torino)

### Session 7: Tutorial 6
4:00 PM – 5:00 PM · Synergy 1 · Chair: Rajen Murugan

4:00 PM **Electromagnetic Modeling of 3D Integrated Circuits with Integral Equation Methods**
*Piero Triverio* (University of Toronto)

# Monday, October 19, 2026

## Session 8: Welcome Remarks
9:00 AM – 9:10 AM · Synergy 1 · Chair: Xu Chen

## Session 9: Keynote 1
9:10 AM – 10:10 AM · Synergy 1 · Chair: Xu Chen

9:10 AM — **AI Meets Chips and Packaging: From Prediction to Generation**
*David Z. Pan* (The University of Texas at Austin)

## Session 10: Modeling and Simulation
10:10 AM – 11:10 AM · Synergy 1 · Chair: Piero Triverio

10:10 AM #31 — **Constraining Poles of Parameterized Macromodels**
*Antonio Carlucci, Tommaso Bradde and Stefano Grivet-Talocia* (Politecnico di Torino)

10:30 AM #58 — **An Efficient NN Architecture for Harmonic Balance-based Analysis for SI Applications**
*Anuj Mathur and Ahsan Javaid* (Carleton University)*; Vinay Suresh Rao* (Marvell)*; Dani Tannir* (Lebanese American University)*; Zohreh Naghibi and Ramachandra Achar* (Carleton University)

10:50 AM #56 — **Deep Equilibrium Recurrent–Transformer (DERT) Model for Large Coupled Interconnect Systems**
*Ahsan Javaid, Anuj Mathur and Ramachandra Achar* (Carleton University)

**11:10 AM – 11:30 AM · Coffee Break · Pre-Function (5th Floor)**

## Session 11: APAC Special Panel Session
11:30 AM – 12:30 PM · Synergy 1 · Chair: Yutaka Uematsu

## Session 12: TPC Meeting
12:30 PM – 2:00 PM · Synergy 3 · Chair: Xu Chen

**12:30 PM – 2:00 PM · Lunch Break**

## Session 13: Packaging Research from APAC Region
2:00 PM – 3:20 PM · Synergy 1 · Chair: Yutaka Uematsu

2:00 PM #5 — **Thermal-Aware Signal Integrity Analysis of GPU-HBM-HBF Interposer Channels Considering HBF Power Consumption**
*Gwantaek Lee, Junghyun Lee, Youngsu Yoon, Jiwon Yoon, Byeongmok Kim, Junho Park, Jaegeun Bae, Hyunjun An, Haeseok Suh, Chaemin Yang, Seungjae Lee and Joungho Kim* (Korea Advanced Institute of Science and Technology (KAIST))

2:20 PM #39 — **Transformer-Based S-Parameter Prediction for Chiplet Interconnects with Sparse Global Context**
*Pin-Yuan Yang, Cheng-Wei Liu and Shih-Chieh Chang* (National Tsing Hua University)

2:40 PM #21 — **Physics-Guided Wideband S-Parameter Prediction for UCIe Interconnect Using Resonance-Aware Gaussian Process Regression**
*Soshi Shimomura, Akiyasu Miyamoto, Takashi Hamaguchi, Takashi Ikeguchi and Yutaka Uematsu* (Hitachi Ltd)

## Session 14: Keysight Demonstration Presentation
3:00 PM – 3:10 PM · Synergy 1 · Chair: Xu Chen

**3:10 PM – 3:40 PM · Coffee Break · Pre-Function (5th Floor)**

## Session 15: Machine Learning for Interconnect Modeling
3:40 PM – 5:00 PM · Synergy 1 · Chair: Stefano Grivet-Talocia

3:40 PM #18 — **Data-Efficient Training of Machine Learning Surrogates with Application to a Memory Interposer**
*Michele Cusano and Paolo Manfredi* (Politecnico di Torino)*; Xuan Chen* (Advanced Micro Devices, Inc.)*; Piero Triverio* (University of Toronto)

4:00 PM #50 — **Pattern- and Channel-Aware Physics-Assisted Deep Learning for Per-DQ Eye-Metric Estimation in RDL Interposer Channels**
*Hyungho Cho, Jaegeun Bae, Junghyun Lee, Haeseok Suh, Chaemin Yang, Gwantaek Lee, Seungjae Lee and Joungho Kim* (Kaist)

4:20 PM #34 — **Machine-Learning-Based Multi-Channel Optical I/O Analysis for Co-Packaged Optics**
*Dekang Chen, Yalong Gu, Duye Ye, Zhichao Zhang and Kemal Aygün* (Intel Corporation)

4:40 PM #44 — **Physics-Derived Machine Learning Surrogate Modeling for Rapid LPDDR Signal Integrity Triage**
*Venkat Satagopan* (NVIDIA Corporation)*; Ram Krishna* (University of Illinois, Urbana-Champaign)*; Clement Luk and Karthik Mahesh Rao* (NVIDIA Corporation)

## Session 16: Poster Session

5:00 PM – 6:30 PM · Pre-Function (7th Floor) · Chair: Tina Bao

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| #25 | **Design Optimization for 224Gb/s Channel in High Density Interconnect Printed Circuit Boards**<br>*Mengen Zan, Chen Cheng, Fanhua Meng and Xinyi Hu* (New H3C)*; Huafang Ju and Jimmy Hsu* (Intel Corporation) |
| #7 | **Active-Learning-Based TX FIR Tuning for High-Speed Links Under Dynamic Thermal Ramping**<br>*Jiazhen Li, Ronnie Zheng and Peng Fu* (Ericsson (China) Communications Co., Ltd.) |
| #11 | **AI-Assisted Chiplet Design Space Exploration with Physics-Aware Reduced-Order Modeling**<br>*Yutaka Uematsu, Takashi Hamaguchi, Soshi Shimomura, Yu Harubeppu, Kisho Ashida and Akiyasu Miyamoto* (Hitachi Ltd.) |
| #12 | **Signal and Power Integrity Analysis of 32 Gbps Die-to-Die Interconnects for Chiplet**<br>*Shengjuan Zhou* (International Innovation Center of Tsinghua University,Shanghai)*; Qian Wang and Jian Cai* (School of Integrated Circuits Tsinghua University) |
| #20 | **SI/PI Trade-off Analysis of UCIe-A Interfaces Considering Power/Ground-to-Signal Bump Ratios**<br>*Seungjae Lee, Junghyun Lee, Hyunjun An, Byeongmok Kim, Haeseok Suh, Youngsu Yoon, Jiwon Yoon, Chaemin Yang, Gwantaek Lee and Joungho Kim* (Korea Advanced Institute of Science and Technology) |
| #22 | **Design and Analysis of HBM-HBF-NMC Architecture for LLM Inference Considering Signal Integrity**<br>*Chaemin Yang, Jiwon Yoon, Haeseok Suh, Junghyun Lee, Hyunjun An, Junho Park, Byeongmok Kim, Youngsu Yoon, Hyuni Lee, Gwantaek Lee, Seungjae Lee and Joungho Kim* (Korea Advanced Institute of Science and Technology (KAIST)) |
| #24 | **Package-level thermal optimization for high-power-density AI accelerators**<br>*Sushil Panda and Paul D. Franzon* (North Carolina State University) |
| #28 | **Influence of Interface Roughness Between Ag Sintered Bonding Layer and Cu on Thermal Stress in SiC Power Chip System with AMB Substrate**<br>*Sean Ogawa, Masaaki Aoki, Akio Iwabuchi, Toshiki Kunieda and Nobuhiko Nakano* (Keio University) |
| #38 | **8533 MT/s LPDDR5X Package Design with Memory-on-Board Topology**<br>*Jeffrey Majnaric, Tingdong Zhou, Geetansh Arora and Robert Wenzel* (NXP) |
| #40 | **Extension of a 2D CIM-Based Approach for Efficient and Automated Computation of Resistances for DC-Analysis of Multilayer PCBs**<br>*Mathis Tobaben, Jan Hessling and Christian Schuster* (Hamburg University of Technology) |
| #46 | **Physics-Aware Reinforcement Learning for Timing-Margin Optimization of High-Speed DDR5 RDIMM**<br>*Changhyun Jung* (TeraByte Interconnection and Package Laboratory, KAIST)*; Seungjae Lee* (Korea Advanced Institute of Science and Technology (KAIST))*; Haeseok Suh* (TeraByte Interconnection and Package Laboratory, KAIST)*; Jaegeun Bae, Gwantaek Lee and Chaemin Yang* (Korea Advanced Institute of Science and Technology (KAIST))*; Joungho Kim* (TeraByte Interconnection and Package Laboratory, KAIST) |
| #48 | **Immersion Cooling Fixture for High Power Testing of Planar Microwave Transmission Lines**<br>*Mohammad Sanad Altaher and Thomas Weller* (University of Nevada, Reno) |

**5:00 PM – 6:30 PM · Welcome Reception · Atrium (7th Floor)**

# Tuesday, October 20, 2026

## Session 17: Keynote 2
9:00 AM – 10:00 AM · Synergy 1 · Chair: Xu Chen

9:00 AM — **Circuits and Packaging for Next Generation AI Datacenters**
*C. Thomas Gray* (NVIDIA)

## Session 18A: AI for Electronic Design Automation
10:00 AM – 11:00 AM · Synergy 1 · Chair: Paolo Manfredi

10:00 AM #33 — **Efficient Agentic Touchstone Analysis via DSL**
*Stefan De Araujo, Bhyrav Mutnury and Arun Chada* (AMD)

10:20 AM #49 — **PDGBench: A Multimodal Fine-Tuning Dataset for Product Design Guide Image Comprehension**
*Nirjhor Rouf* (North Carolina State University); *Priyank Kashyap* (Hewlett Packard Enterprise); *Soumyadeep Chatterjee* (North Carolina State University); *Yuejiang Wen* (Hewlett Packard Enterprise); *Paul D. Franzon* (North Carolina State University)

10:40 AM #19 — **Bayesian Optimization of Crossbar-Based Compute-In-Memory System Design for Efficient DNN Inference**
*Arnob Saha* (Penn State University); *Bibhas Manna* (NIT Meghalaya); *Nikhil Kotikalapudi and Md Zesun Ahmed Mia* (Penn State University); *Rahul Kumar* (Ansys); *Madhavan Swaminathan and Abhronil Sengupta* (Penn State University)

## Session 18B: Keysight SI vs. PI Simulation to Measurement Presentation
10:00 AM – 10:30 AM · Synergy 3

**11:00 AM – 11:20 AM · Coffee Break · Pre-Function (5th Floor)**

## Session 19: Heterogeneous Integration and HBM
11:20 AM – 12:20 PM · Synergy 1 · Chair: Ram Achar

11:20 AM #45 — **Cost-Aware Design Space Exploration of Yield-Compliant UCIe Interconnects**
*Ram Krishna* (University of Illinois, Urbana-Champaign); *Ashita Victor* (Georgia Institute of Technology, Atlanta); *Michael Molter* (University of illinois Urbana Champaign); *Xu Chen* (University of Illinois at Urbana-Champaign); *Muhannad S. Bakir* (Georgia Institute of Technology); *Elyse Rosenbaum* (University of Illinois Urbana Champaign)

11:40 AM #6 — **Signal Integrity Design and Optimization of High-Bandwidth Memory Test System**
*Mohammed Farhan Ahmed, Karsten Klarqvist, Nick Goralka, Yunhui Chu, Ataul Karim, Yen Chun Lee and Chanz Murata* (Micron Technology Inc. USA)

12:00 PM #23 — **Dual-Referenced Circuit Ports for Hybrid Modeling and Correlation of HPC Memory Interfaces**
*Yuandong Guo, Xuan Chen, Bhyrav Mutnury, Manjunath Shivappa, Wil Choon Song, Aik Hong Tan and Shutong Qi* (Advanced Micro Devices, Inc.)

## Session 20: Amphenol Sponsor Demonstration
12:20 PM – 12:30 PM · Synergy 1 · Chair: Xu Chen

**12:30 PM – 1:30 PM · Lunch Break**

## Session 21: IEEE TC on EDMS
1:30 PM – 1:40 PM · Synergy 1 · Chair: Heidi Barnes

## Session 22: EPEPS 2027 Announcement
1:40 PM – 1:50 PM · Synergy 1 · Chair: Rajen Murugan

## Session 23: Signal Integrity 1

1:50 PM – 3:10 PM · Synergy 1 · Chair: Rajen Murugan

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| 1:50 PM #42 | **Mitigating the Impact of Glass Weave on Bidirectional High-Speed Signaling**<br>*Hakki M. Torun and Jose A. Hejase* (NVIDIA) |
| 2:10 PM #27 | **A Low-Power, Low-Cost USB4 Cable Using an Ultra-Wideband Signal Integrity Recovery Structure**<br>*Mun-Ju Kim, Byung-Cheol Min, Dong-Jae Go and Kyung-Bin Yoo* (School of Electronic and Electrical Engineering, Kyungpook National University, Daegu)*; Abhijit Wander* (Signal Integrity, Independent Researcher)*; Raheeq Darweesh* (Signal Integrity, Amphenol Communications Solutions)*; Sehoon Park and Kang-Wook Kim* (School of Electronic and Electrical Engineering, Kyungpook National University, Daegu) |
| 2:30 PM #47 | **A Differential Tab Structure Design for Optimizing 200G+ PCB Via Transitions**<br>*Yuting Yeh, Adewale K. Oladeinde and Jose A. Hejase* (NVIDIA Corporation) |
| 2:50 PM #26 | **Balanced Line-based Ultra-wideband Channel with Enhanced SNR for 224G/448G SerDes Links**<br>*Byung Cheol Min, Kang Wook Kim and Mun Ju Kim* (Kyungpook National University)*; Dong Jae Go* (School of Electronic and Electrical Engineering, Kyungpook National University, Daegu)*; Raheeq Darweesh* (Amphenol Communications Solutions)*; Abhijit Wander* (Independent Researcher) |

## Session 24: Amphenol Substrate Design Considerations for Co-Packaged Optics Presenation

2:00 PM – 2:30 PM · Synergy 3

**3:10 PM – 3:30 PM · Coffee Break**

## Session 25: Signal Integrity 2

3:30 PM – 4:50 PM · Synergy 1 · Chair: Heidi Barnes

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| 3:30 PM #43 | **Common-Mode Sign-Based P/N Skew Calibration for 212.5-Gbps PAM-4 Wireline Receivers**<br>*Chiho Song and Samuel Palermo* (Texas A&M University) |
| 3:50 PM #36 | **Voltage Supply Noise Analysis of Phase-Locked Loop (PLL) Structure in Custom Base Die of High Bandwidth Memory (HBM)**<br>*Jaegeun Bae* (KAIST)*; Byeongmok Kim, Haeseok Suh, Jiwon Yoon, Keunwoo Kim, Youngsu Yoon, Junho Park, Hyunjun An, Chaemin Yang, Gwantaek Lee, Seungjae Lee and Joungho Kim* (Korea Advanced Institute of Science and Technology (KAIST)) |
| 4:10 PM #37 | **Impact of Ground Bounce on Logic-HIGH in Differential Signalling: Case Study of a Current-Mode Driver**<br>*Anuj Kumar and Jai Narayan Tripathi* (Indian Institute of technology Jodhpur) |
| 4:30 PM #32 | **Simulation-driven Adaptive Estimation of Worst-case Power Noise**<br>*Davide Covolo, Antonio Carlucci and Stefano Grivet-Talocia* (Politecnico di Torino) |

## Session 26: Power Integrity

4:50 PM – 6:10 PM · Synergy 1 · Chair: Jose Hejase

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| 4:50 PM #8 | **Design of Integrated Voltage Regulators using a Generative Waveform Surrogate**<br>*Md Sultan Mahmud, Ramin Rahimzadeh Khorasani and Madhavan Swaminathan* (The Pennsylvania State University) |
| 5:10 PM #35 | **Equal Source Voltages for Minimum DC Conduction Loss in High-Current Power-Delivery Interconnects**<br>*Hanyu Zhang* (Missouri University of Science and Technology)*; Zhiping Yang* (PCB Automation Inc.)*; Chulsoon Hwang* (Missouri University of Science and Technology) |
| 5:30 PM #55 | **Non-Uniform Channel Allocation in Multi-Fin GaN Tri-Gate Transistors for Package-Integrated Power Delivery**<br>*Ayoub Sadeghi* (PhD Student, University of Illinois Chicago)*; Sohrab Sheikh Sofla and Madhavan Swaminathan* (Pennsylvania State University, State College, PA, USA)*; Inna Partin-Vaisband* (University of Illinois Chicago, Chicago, IL, USA) |
| 5:50 PM #9 | **Model-Driven Design Exploration of Hybrid Voltage Regulators for Vertical Power Delivery**<br>*Salma Abdelzaher, Mohamed Gharib and Inna Partin-Vaisband* (University of Illinois Chicago) |

**6:10 PM – 8:00 PM · Awards Reception · Atrium (7th Floor)**

# Wednesday, October 21, 2026

## Session 27: Electromagnetics

8:30 AM – 9:30 AM · Synergy 1 · Chair: Kemal Aygun

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| 8:30 AM #17 | **Investigation of Nanowire Crosstalk through an Ab-Initio EM/QM Simulation Framework**<br>*Maxim Torreele, Emile Vanderstraeten and Dries Vande Ginste* (Ghent University) |
| 8:50 AM #53 | **Tensor-Train Accelerated Solution of Three-Dimensional Volume Integral Equations in Modeling of Optical Interconnects**<br>*Chris Nguyen and Vladimir I. Okhmatovski* (University of Manitoba) |
| 9:10 AM #30 | **Fast Electromagnetic Analysis of Multiscale Structures Using MultiAIM with an Improved Projection Scheme**<br>*Yongzhong Li and Piero Triverio* (University of Toronto) |

**9:30 AM – 10:00 AM · Coffee Break · Pre-Function (5th Floor)**

## Session 28: Thermal-Mechanical Analysis

10:00 AM – 11:00 AM · Synergy 1 · Chair: Dries Vande Ginste

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| 10:00 AM #16 | **Component-Based Model Order Reduction of Thermal-Mechanical Analysis for Chiplet Design**<br>*Akiyasu Miyamoto, Takashi Hamaguchi, Soshi Shimomura and Yutaka Uematsu* (Hitachi, Ltd.) |
| 10:20 AM #10 | **Fast Transient Electrothermal Co-Simulation for Thermal-Integrity Analysis of Power-Gated 2.5D/3D Systems**<br>*Mohamed Gharib, Salma Abdelzaher and Inna Partin-Vaisband* (University of Illinois Chicago) |
| 10:40 AM #29 | **Analysis on Creep Strain and Fatigue Resistance of Ag Sintered Bonding Layers in SiC Chip Systems Using Ag Sintering Chip-Attachment**<br>*Toshiki Kunieda, Masaaki Aoki, Akio Iwabuchi and Sean Ogawa* (Keio University)*; Kentaro Yoshioka and Akihiro Mochizuki* (MacDermid Performance Solutions Japan)*; Nobuhiko Nakano* (Keio University) |

## Session 29: RF and Quantum Interconnects

11:00 AM – 12:30 PM · Synergy 1 · Chair: Vladimir Okhmatovski

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| 11:00 AM #57 | **Systematic Synthesis of Ultra-Compact On-Chip E-Band 360° Phase Shifter**<br>*Han-Ting Lin and Andreas Weisshaar* (Oregon State University) |
| 11:20 AM #4 | **Improved Signal Integrity Modeling for Quantum Flex Circuits via Low-Temperature Dk/Df Extraction**<br>*Madeleine Guo* (AMD, San Jose, CA)*; George Paulik, Abel Tesfai, Dylan Grace and Matt Doyle* (IBM, Rochester, MN) |
| 11:40 AM #51 | **Rooftop SSPP Interconnect with Filtering and Crosstalk Suppression at Cryogenic State (77 K)**<br>*Md. Omar F. Noman and Soumitra Joy* (University of North Carolina at Charlotte) |
| 12:00 PM #52 | **Harvesting Waste Heat for Autonomous Reconfigurability in VO2-Based spSIW Interconnect**<br>*Abdelrahman Omar and Soumitra Joy* (University of North Carolina at Charlotte) |

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