



The Design and Analysis Frontier of Electronic Packaging

31st Conference on Electrical Performance of Electronic Packaging and Systems

October 9th to 12th, 2022



Call for Papers



EPEPS is the premier international conference on advanced and emerging issues in electrical modeling, measurement, analysis, synthesis, and design of electronic interconnections, packages, and systems. It also focuses on new methodologies and CAD/design techniques for evaluating signal, power, and thermal integrity and ensuring performance in high-speed, RF, and wireless designs. EPEPS is jointly sponsored by IEEE Electronics Packaging Society, IEEE Microwave Theory and Techniques Society, and IEEE Antennas and Propagation Society. Submitted papers should describe new technical contributions related to the area of the electrical performance of high-performance interconnect systems, covering:

- System-level, board-level, package-level and on-chip interconnects
- High-speed channels, links, backplanes, serial and parallel interconnects, SerDes
- RF/microwave/mm-wave packaging structures and components, antenna-in-package and RFIC co-design, mixed signal modules and wireless switches
- Signal and thermal integrity
- Power integrity and power distribution networks
- Low power mobile and personal applications
- Memory and DDR interfaces
- Jitter and noise management
- Electronic packages and microsystems
- Heterogeneous integration, 2.5D/3D interconnects and packages, TSVs and MCMs
- Electromagnetic (EM) and EM interference modeling, simulation algorithms, tools, and flows
- Macro-modeling and model order reduction as it applies to electrical analysis
- Advanced and parallel CAD techniques for signal, power, and thermal integrity analysis
- Measurement and data analysis techniques for system-level and on-chip structures
- High volume testing for electronic packages.

Submission Deadline: July 24, 2022

Conference Chairs:

Zhen Peng, zvpeng@illinois.edu

Swagato Chakraborty, Swagato_Chakraborty@mentor.com

For more information/contact: epeps-admin@illinois.edu

Submission Format: 2-column, 3-page PDF format only.

Selected papers will be invited for a special issue in *IEEE Transactions on Components, Packaging, and Manufacturing Technology*. Information for authors can be found at www.epeps.org. Submitted manuscripts should be camera-ready and compliant with the general standards of the IEEE, including appropriate referencing. Noncompliant manuscripts will not be considered for review.

Location: San Jose Marriott, 301 South Market Street, San Jose, CA 95113, USA.

Tutorials: EPEPS offers tutorials on state-of-the-art topics including latest advances: on CAD software tool techniques for package/PCB design, SI and PI modeling, high-speed SerDes simulation, high precision measurement techniques and novel interconnect design.

IEEE Education Credits: IEEE offers professional development hours (PDHs) and continuing education units (CEUs) for attending the EPEPS program.

Simulation Benchmarking: EPEPS 2022 organizers invite paper submissions covering simulation tool development advances that utilize benchmarks established and released publicly by the IEEE TC-EDMS Packaging Benchmarks Committee (<http://www.packaging-benchmarks.org/>).

Exhibits: EPEPS offers an excellent array of vendor exhibits. EPEPS is an exciting forum for vendors to demonstrate their state-of-the-art tools to attendees. Interested vendors can contact the conference administration for more details.

Conference Website: www.epeps.org